EDITED BY BILL TRAVIS & ANNE WATSON SWAGER

Battery simulator provides current limiting

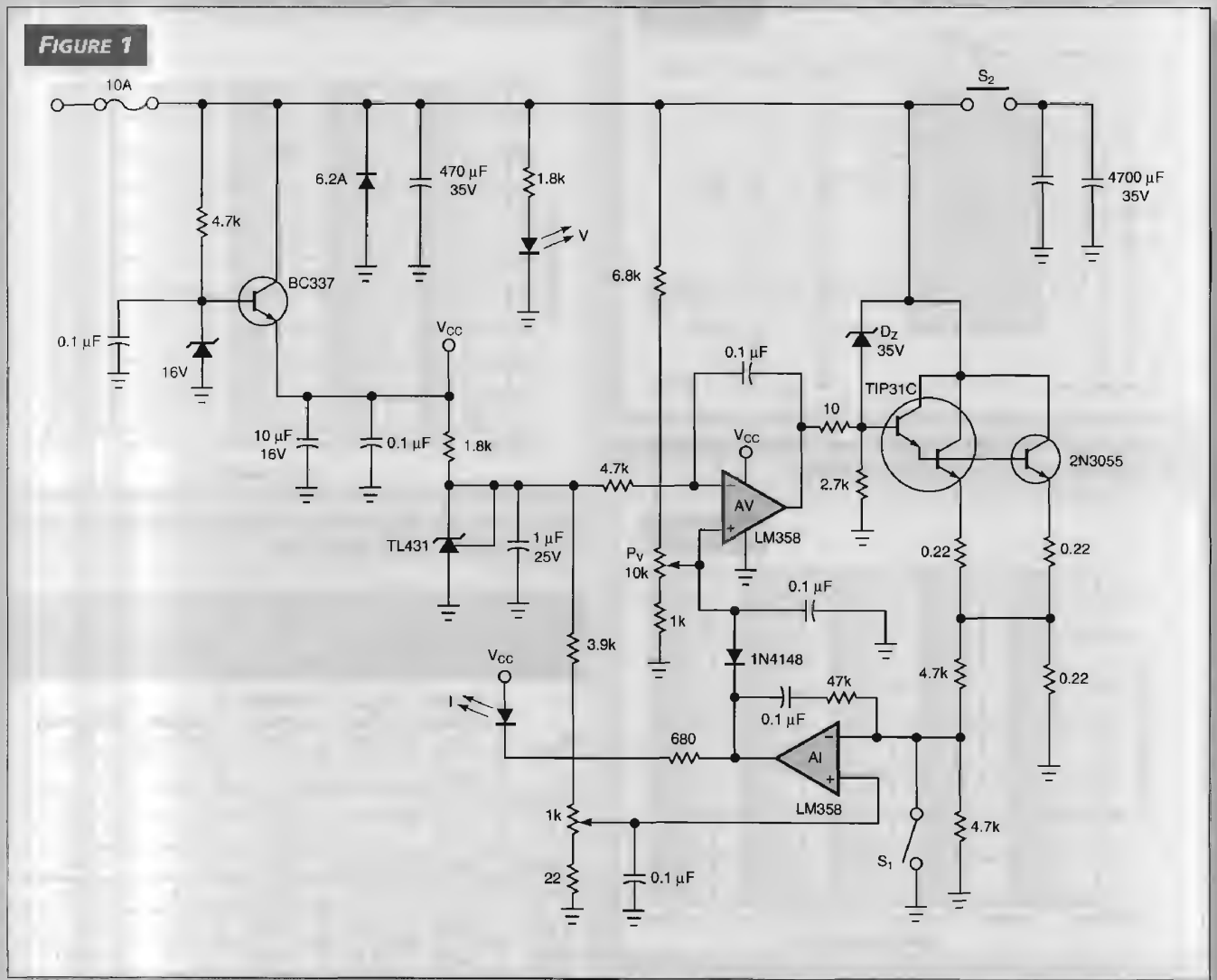
HERNAN TACCA, UNIVERSITY OF BUENOS AIRES, ARGENTINA

A constant-voltage active load can perform as a battery during the charge cycle (**Figure 1**). You can set the load voltage from 5 to 35V by using potentiometer P_v and thus can simulate batteries ranging from 6 to 32V. In testing a battery charger (during design or for calibration purposes), a current-limiting function is a desirable feature; you enable this protection feature by opening S_1. The LED lights if the current reaches the limit. This feature lets you know when the circuit goes out of its constant-voltage operating mode.

To simulate the dynamic behavior of a battery, you can connect several electrolytic capacitors. With the addition of these capacitors, current pulses can flow bidirectionally between the load and the battery charger. In some cases, a large capacitive load could cause oscillations, making it difficult to provide loop compensation for stable closed-loop operation. In case of such instability, switch S_2 provides capacitor disconnection. If you encounter closed-loop compensation problems, try to compensate without using capacitors. (DI #2065) EDN

To Vote For This Design, Circle No. 376

FIGURE 1



A battery-simulation circuit comes in handy when you're designing battery chargers.

Inverter forms high-efficiency rail-splitter

TERRY MILLWARD, MAXIM INTEGRATED PRODUCTS, READING, UK

In **Figure 1**, a switched-capacitor voltage inverter, IC_1, configured as a "rail-splitter," provides a bipolar, dual-rail power supply. The circuit is useful in single-supply systems that include one or more dual-supply ICs. The SOT-23 package and associated components require little board area. After you apply power, the flying capacitor, C_2, connects alternately across the storage capacitors, C_3/C_4 and C_5/C_6. This operation equalizes the voltages on those capacitors and draws current from V_{IN} or V_{OUT} as required to maintain $V_{OUT}=½V_{IN}$.

If the loads across $V_{IN}–V_{OUT}$ and $V_{OUT}–0V$ are equal, the IC remains in a quiescent state and draws approximately 36 µA. To keep V_{OUT} at the midrail level, the flying capacitor need only supply the difference current arising from unbalanced loads. The IC's quiescent current dominates the efficiency for load currents less than 100 µA, but for currents greater than 1 mA, the efficiency is greater than 90%—an important feature for low-power or battery-powered systems. The voltage error and efficiency vary with the load current (**Figures 2** and **3**).

This switched-capacitor circuit provides better regulation than that of a simple voltage divider and better efficiency than that of a simple combination of a divider and an op-amp buffer. The circuit's main drawback is the increase in output noise with load (**Table 1**). V_{IN} is limited to the maximum voltage allowed between pins 2 and 4 or between pins 1 and 4; that is, 5.5V. (DI #2054) EDN

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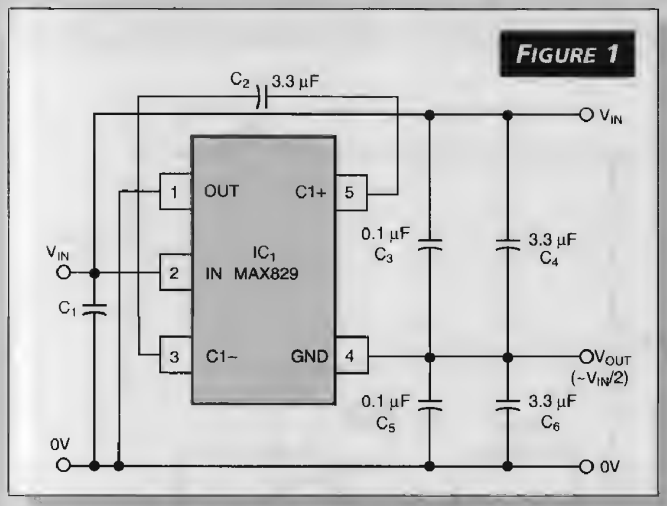
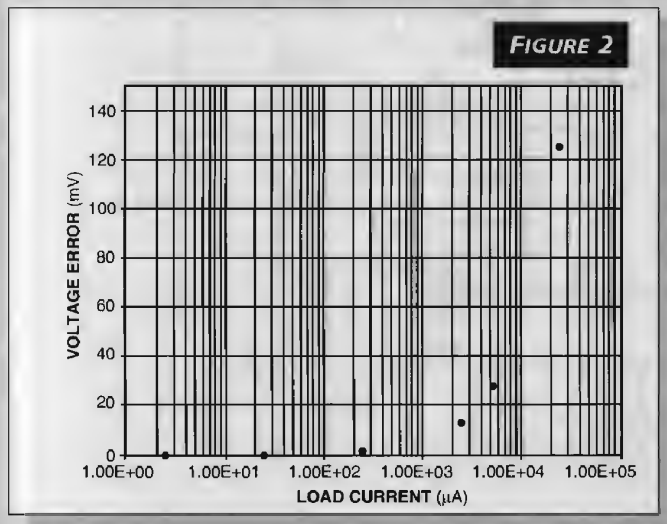
FIGURE 1



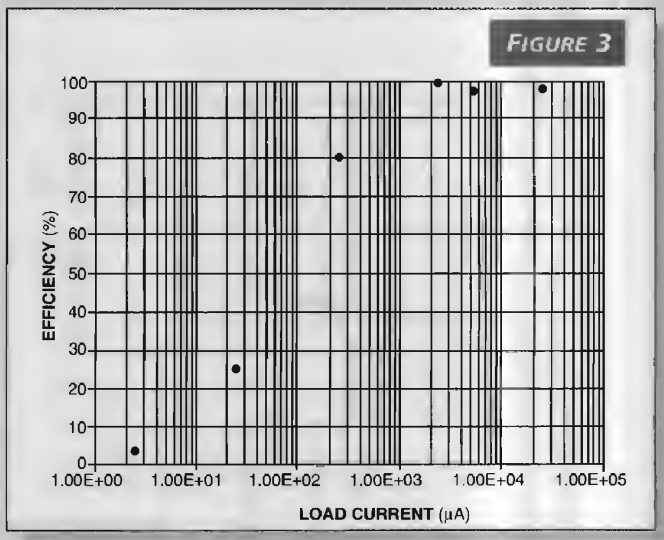
A compact and efficient charge-pump circuit implements a local dual-rail supply in single-rail systems.

FIGURE 2



Output-voltage error for the circuit in Figure 1 increases as a function of load current.

FIGURE 3



For load currents greater than 1 mA, the efficiency for the circuit in Figure 1 is well above 90%.

TABLE 1—RAIL-SPLITTER PERFORMANCE FOR V_{IN}=5V

R_{LOAD}	Input current (µA)	V_{OUT} error (mV)	Output current (µA)	Ripple (mV p-p)	Efficiency (%)
∞	36.5				
10 MΩ	36.5		0.25		0.34
1 MΩ	36.7		2.5		3.32
100 kΩ	48.9	0.1	25		25.56
10 kΩ	156	1.4	250	1	80.04
1 kΩ	1240	13.5	2490	5	99.72
470Ω	2630	28.5	5260	8	98.83
100Ω	11,410	126.9	23,700	30	98.71

Add trimmable current limit to dc/dc supply

TERRY MILLWARD, MAXIM INTEGRATED PRODUCTS UK LTD, THEALE, UK

You can add a simple, two-transistor circuit to a standard, step-down dc/dc converter to provide an adjustable limit for the output current (**Figure 1**). You can apply this method to most step-down converters that provide access to the feedback node. The circuit uses a PWM switch-mode regulator, IC_1, to generate 9V from an input of 12 to 30V (a range that satisfies automotive applications). R_4 senses the output current; the current limit is $0.65/R_4$, which in this case is 440 mA. The limiting current produces sufficient voltage across R_4 to turn on Q_2.

The current through R_2 then turns on Q_1, which throttles the output current by sourcing current to the feedback node on Pin 8. R_3 protects Q_2's base-emitter junction in the event of an output short circuit. Because R_5 and R_6 sense the output voltage downstream from the current-sense resistor, V_{OUT} stays in regulation until the current reaches the limit. This regulation characteristic is useful in battery-charging applications. R_5 and R_6 set the regulated output level according to

$$V_{OUT} = \frac{2.21(R_5 + R_6)}{R_6}.$$

(DI #2062)

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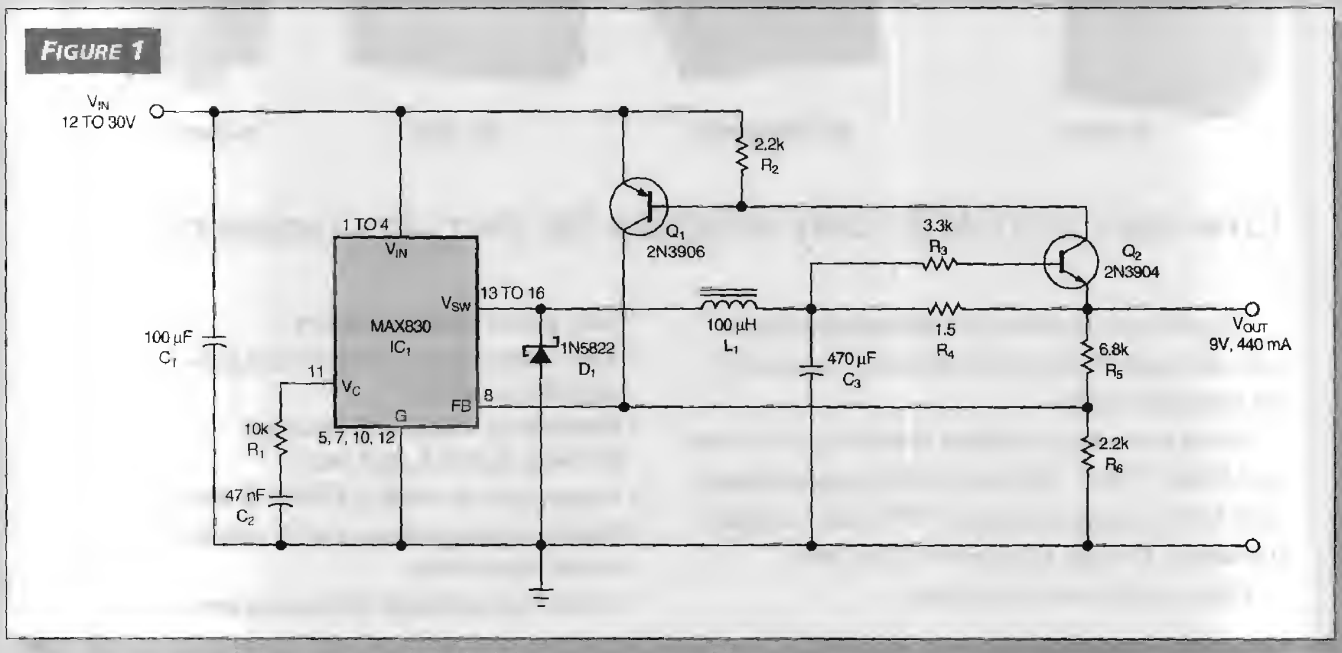
FIGURE 1



Adding two transistors allows this standard switch-mode buck regulator to limit the output current to $0.65/R_4$.

µC controls charge pump as background task

CARLOS COSSIO, SANTANDER, SPAIN

Because of power consumption and cost, designers of battery-powered devices mainly choose components that run at 3V or lower. Unfortunately, many devices operate only at 5V, including LCDs with built-in drivers, programming lines of many EEPROMs and flash chips, and CMOS ADCs. You thus need a small, inexpensive dc/dc converter to supply the 5V. If your system uses a low-cost µC, you can use some µC resources (two high-current I/O pins, a timer, and a software trick) and a few external components (two diodes and two capacitors) to build an inexpensive charge pump (**Figure 1**). The pump runs as a background software task to generate the needed 5V.

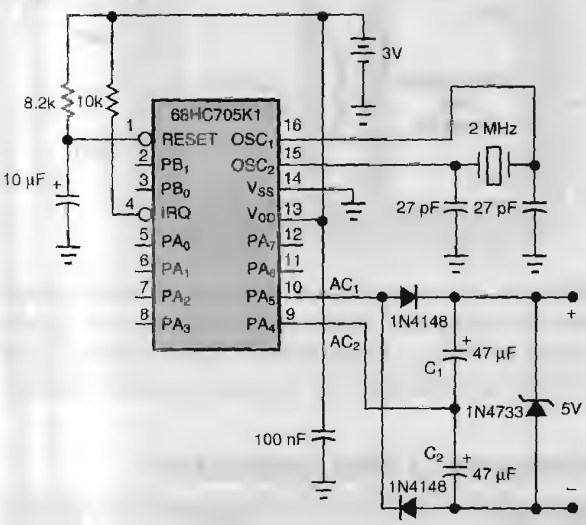
Because the charge pump uses a full-wave voltage doubler, it's necessary to generate in software an ac signal of +3 to –3V that is capable of charging every capacitor to 3V. To obtain this type of signal using a µC powered only by 3V, it's neces-

sary to change the ground voltage you apply to the common or reference alternately between AC_1 and AC_2. That is, to obtain a positive half-cycle of 3V, the AC_1 pin must pull up to 3V while the AC_2 pin pulls down to 0V. Similarly, to obtain a negative half-cycle of –3V, the AC_1 pin must pull down to 0V, and the AC_2 pin must pull up to 3V. The result is a square wave that alternates between 3 and –3V (**Figure 2**).

Capacitor C_1 charges during the positive half-cycle of the signal, and capacitor C_2 charges during the negative half-cycle. Thus, for light loads, the output voltage from both capacitors is approximately 6V. If you need a regulated 5V output, you can insert a zener diode to clamp the voltage at 5V. The assembly code in **Listing 1** applies to Motorola's (Phoenix, AZ) low-cost MC68HC705K1 µC. The software uses the µC's periodic-timer interrupt capability every millisecond to obtain a 500-Hz frequency, a rate low enough to fully charge C_1 and C_2 without compromising system performance. (You can download **Listing 1** from *EDN*'s Web site, www.ednmag.com. At the registered-user area, go into the Software Center to download the file from DI-SIG, #2063.)

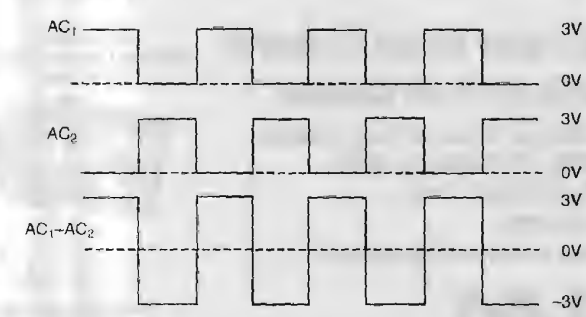
You can effect a shutdown feature if you disable the timer interrupt during the program execution. You can thus save battery life by turning off the charge pump when the device requesting 5V is idle. (DI #2063)

FIGURE 1



By alternately switching two µC pins between 0 and 3V, the charge pump generates a net 6V-difference signal.

FIGURE 2



A low-cost µC can control an inexpensive 3 to 5V charge pump as a software background task.

LISTING 1—ASSEMBLY CODE FOR CHARGE-PUMP BACKGROUND TASK

```
**********************************************************************
* This sample program demonstrates how to build a cheap charge-pump  *
* embedded in a microcontroller system as a background task done in   *
* software                                                            *
**********************************************************************

#BASE       $0A                     ;Change default base to decimal

MOR         EQU     $0017           ;Mask Option Register
RAM         EQU     $00E0           ;Beginning of RAM memory
ROM         EQU     $0200           ;Beginning of ROM memory
VECTORS     EQU     $03F8           ;Interrupt vectors

DRA         EQU     $0000           ;Port A Data Register
DDRA        EQU     $0004           ;Port A Data Direction Register
ISCR        EQU     $000A           ;IRQ Status and Control Register
IRQE        EQU     7               ;External interrupt request enable
TSCR        EQU     $0008           ;Timer Status and Control Register
TOFR        EQU     3               ;Timer Overflow Flag Reset

AC1         EQU     5               ;Charge-pump AC input 1
AC2         EQU     4               ;Charge-pump AC input 2

**********************
* MOR byte definition *
**********************
            ORG     MOR

            FCB     $00             ;COP watchdog disabled

**********************
* Program definition *
**********************
            ORG     ROM

            BSET    AC1,DDRA        ;AC1 pin as output
            BSET    AC2,DDRA        ;AC2 pin as output

            BSET    AC1,ORA         ;AC1 set to +3 volts
            BCLR    AC2,ORA         ;AC2 set to 0 volts

            BCLR    IRQE,ISCR       ;Disable IRQ interrupts

            LOA     #%00100000      ;Timer overflow interrupt enabled
                                    ;RTI interrupt disabled
            STA     TSCR            ;Store it
            CLI                     ;Enable interrupts
MAIN
                                    ;Your MAIN code here
            BRA     MAIN

**********************************************************************
* Timer Overflow Interrupt Service Routine executed every 1 msec *
**********************************************************************
CHARGE
            BSET    TOFR,TSCR       ;Reset timer overflow interrupt
            LOA     DRA             ;Get last output latch
            EOR     #%00110000      ;Complement values on AC1 & AC2
            STA     DRA             ;Update signal (frequency 500 Hz.)
DUMMY
            RTI

**********************
* Interrupt Vectors *
**********************
            ORG     VECTORS

            FDB     CHARGE          ;RTI vector
            FDB     DUMMY           ;IRQ vector
            FDB     DUMMY           ;SWI vector
            FDB     MAIN            ;RESET vector

            END
```

To Vote For This Design, Circle No. 379

Use RS-232C port to measure pressure

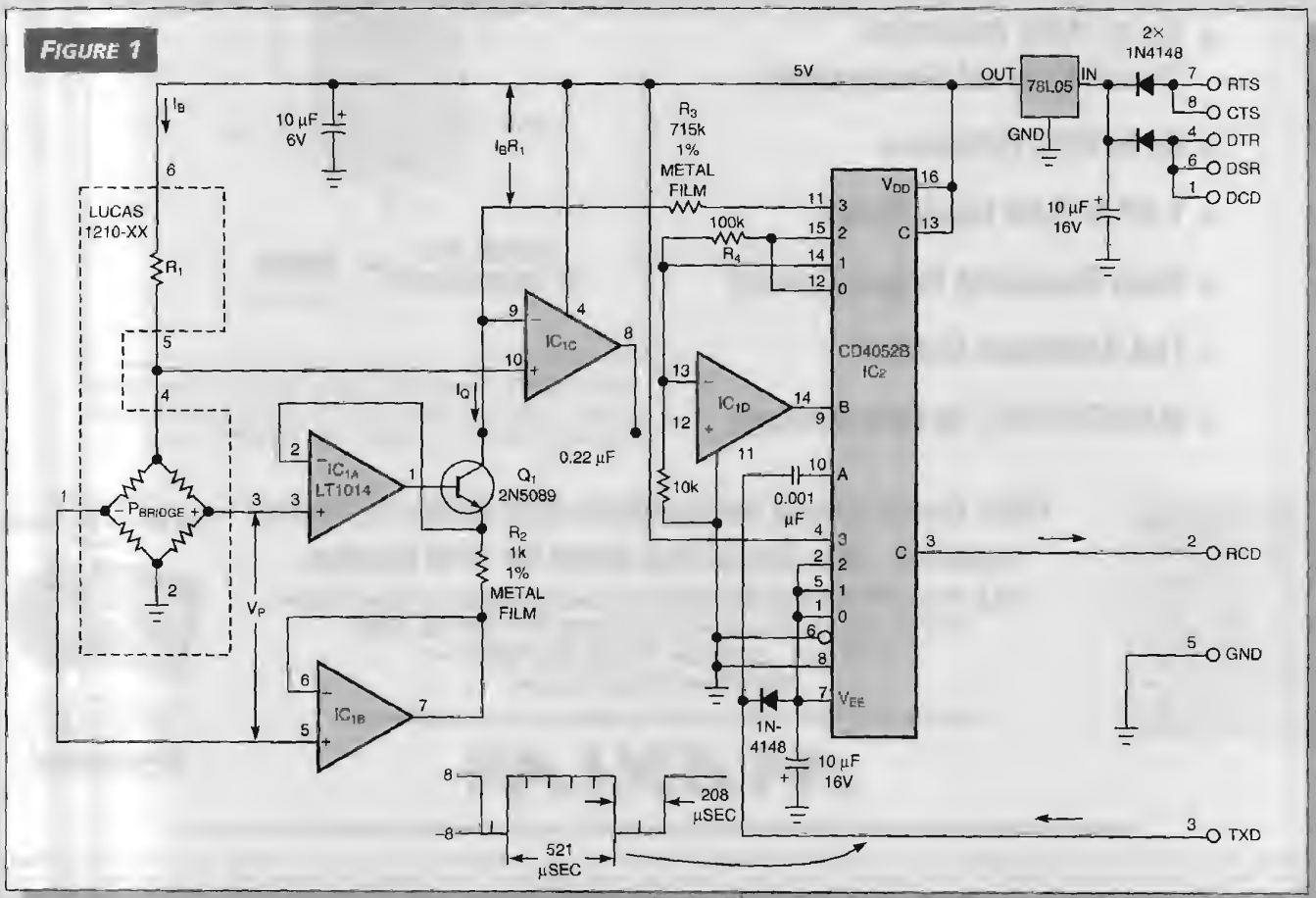
W STEPHEN WOODWARD, UNIVERSITY OF NORTH CAROLINA—CHAPEL HILL

A simple circuit (**Figure 1**) and accompanying software turn a pressure sensor into an accurate and cheap pressure digitizer that works with any PC's RS-232C COM port. Many manufacturers make micromachined silicon piezoresistive pressure sensors. Sensors are available with full-scale sensitivities ranging from inches of water to hundreds of pounds per square inch. A particularly useful breed of these sensors has temperature-compensated outputs proportional to the product of applied pressure and excitation current. This feature makes these sensors suitable for ratiometric operation and accurate functioning with a range of supply voltages. The **figure** uses a handy example from this group: the Lucas Novasensor (Fremont, CA) family. This series of sensors undergoes factory calibration to a range of differential or absolute pressures, and the sensors incorporate on-chip gain-setting resistors that promote trim-free interchangeability.

Electrically, the sensor is equivalent to a strain-gauge bridge biased by R_1, the on-chip gain-setting resistor. Pressure-induced mechanical strain in the silicon of the piezoresistive bridge produces a pressure-proportional differential signal $V_P=P\times S\times I_B$, in which S is the sensor's sensitivity, P is the applied pressure, and I_B is the bias current. IC_{1A} and IC_{1B} sense V_P. Integrator IC_{1C} accumulates the resulting Q_1 collector current, causing its output to ramp up. The collector current is equal to:

$$I_Q = \frac{V_P}{R_2} = \frac{P \bullet S \bullet I_B}{R_2}.$$

Comparator IC_{1D} combines with a dual CD4052B multiplexer, IC_2, to close the feedback loop around IC_{1C} by periodically connecting R_3 to 5V. When this connection happens, the current through R_3 into the integrator equals



A simple circuit and accompanying software turn a pressure sensor into an accurate and cheap pressure digitizer that works with any PC's RS-232C COM port.

$I_B \times R_1/R_3$. If d equals IC_2's duty cycle for integrator balance, then

$$d = \frac{P \bullet S \bullet I_B / R_2}{I_B \bullet R_1 / R_3} = P \bullet \frac{S}{R_1} \bullet \frac{R_3}{R_2}.$$

Factory calibration sets S/R_1 equal to 1/(1000×full-scale psi), so

$$d = \frac{P}{\text{FULL-SCALE PSI}} \bullet \frac{R_3}{1000 \bullet R_2}.$$

Seven-bit binary characters, including start/stop bits, with the pattern of 0000011, drive the conversion. The PC's COM port transmits these characters on TXD at 9600/7, or 1371 Hz. With the start of each character, IC_2 samples the state of IC_{1D}'s output. If this output is low, which indicates integrator balance, IC_2 goes into State 1 of its four possible states. This state shorts R_4, which latches IC_{1D} low for the remainder of the character time. Meanwhile, State 1 holds RCD negative, so the COM port receives no characters.

If, however, IC_{1D}'s output is high, which indicates integrator imbalance, IC_2 goes to State 3, which latches IC_{1D} high. This action connects R_3 to 5V, which nudges the integrator toward balance, and drives RCD to 5V, which echoes the 0000011 character to the COM port. Because TXD has a 5-out-of-7 high/low pattern, the maximum value of d is 5/7, and the best choice for R_3/R_2 equals $S/R_1 \times 5/7 = 1000 \times 5/7 = 714$. This ratio causes the fraction of characters echoed back to the port to range from 0 to 100% as the pressure ranges from 0 to full-scale psi.

The sensor program computes this average frequency as a fraction of 9600 Hz/7×0.979 sec=1342 and converts the result into a pressure reading by multiplying it by the appropriate full-scale factor. (You can download the program from *EDN*'s Web site, www.ednmag.com. At the registered-user area, go into the "Software Center" to download the file from DI-SIG, #2061.) Conversion resolution is proportional to conversion time and is greater than 10 bits (1 part in 1342) in 1 sec, as illustrated in the listing, and 12 bits in 3 sec. (DI #2061)

To Vote For This Design, Circle No. 380

Autotransformer regulator inverts 12V to produce –12V

DANA DAVIS, MAXIM INTEGRATED PRODUCTS, SUNNYVALE, CA

You can create a dc/dc regulator with an internal switching MOSFET that inverts 12V to produce an output of 200 mA at –12V (Figure 1). The IC is a high-efficiency device whose low quiescent current (120 µA maximum) is the product of a CMOS process that limits the absolute-maximum input-to-output voltage to 21V. Thus, to avoid having 24V across its terminals, the IC must isolate itself from the inductor-flyback voltage. It can do so by driving either an external switch in a nonbootstrapped configuration or an internal switch in a flyback-transformer configuration.

Autotransformer T_1, a center-tapped inductor with a 1-to-1 turns ratio, offers a design alternative. Terminal LX flies back to $\frac{1}{2}V_{OUT}$ plus a diode drop, or approximately –6V. The V+ terminal remains at 12V, yielding 18V maximum between V+ and LX—well within the 21V limit. Because IC_1 drives the gate of its internal MOSFET between the V+ and OUT voltages, you normally connect OUT to V_{OUT} to ensure sufficient gate drive. (In a typical application, the chip inverts 5V to produce –5V.) In this circuit, the 12V input provides adequate gate drive, so OUT connects to ground. (DI #2067)

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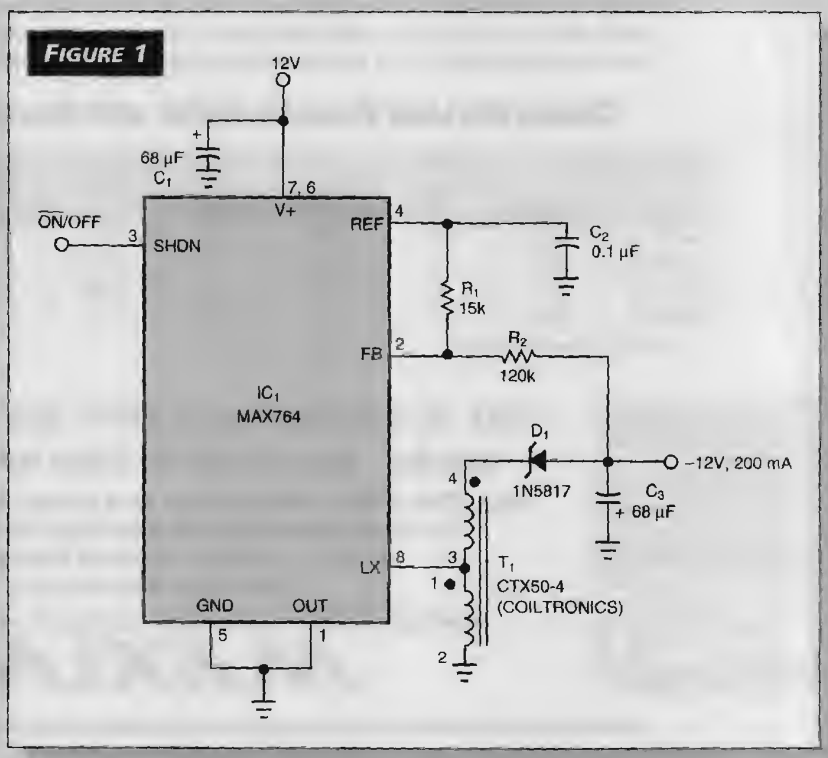
FIGURE 1



Autotransformer T_1 limits the voltage across IC_1, allowing the use of a high-efficiency chip in this inverting dc/dc regulator.

Logic IC yields simple, wide-range timer

HARRY BISSELL JR, ROBOTRON CORP, SOUTHFIELD, MI

You can use a 4060B binary counter/oscillator to make a simple, accurate, long-delay timer (**Figure 1**). The circuit offers longer times (milliseconds to hours) than you can achieve with common IC timers. A positive logic level at the input holds the counters in the reset state and the output in the low state. When the input goes low, the output goes high, forward-biasing D_1 and "stalling" the oscillator. The output then latches in its present state, as the timing diagram shows. The oscillator stops halfway through the count period (when the output switches from low to high), so the turn-off time is a function of the clock period times Q(n–1). Note that the 4060B does not provide a Q_{11} output.

C_1, R_1, and R_2 form a classic two-inverter oscillator. R_1 should have a minimum value of 5 kΩ, with R_2 two to 10 times greater than R_1. Manufacturers' data sheets contain recommendations on minimum and maximum component values. JP_1 is a jumper like those used on computer boards. You can use other methods, but don't allow two output terminals to short together. The state of the counter is not defined at power-up, so the output is usually on. The circuit counts out of this state, or you may use the broken-line optional circuit to prevent an output from occurring until after a valid input appears. As another option, you can capacitively couple the input to form a retriggerable one-shot multivibrator. (DI #2068) EDN

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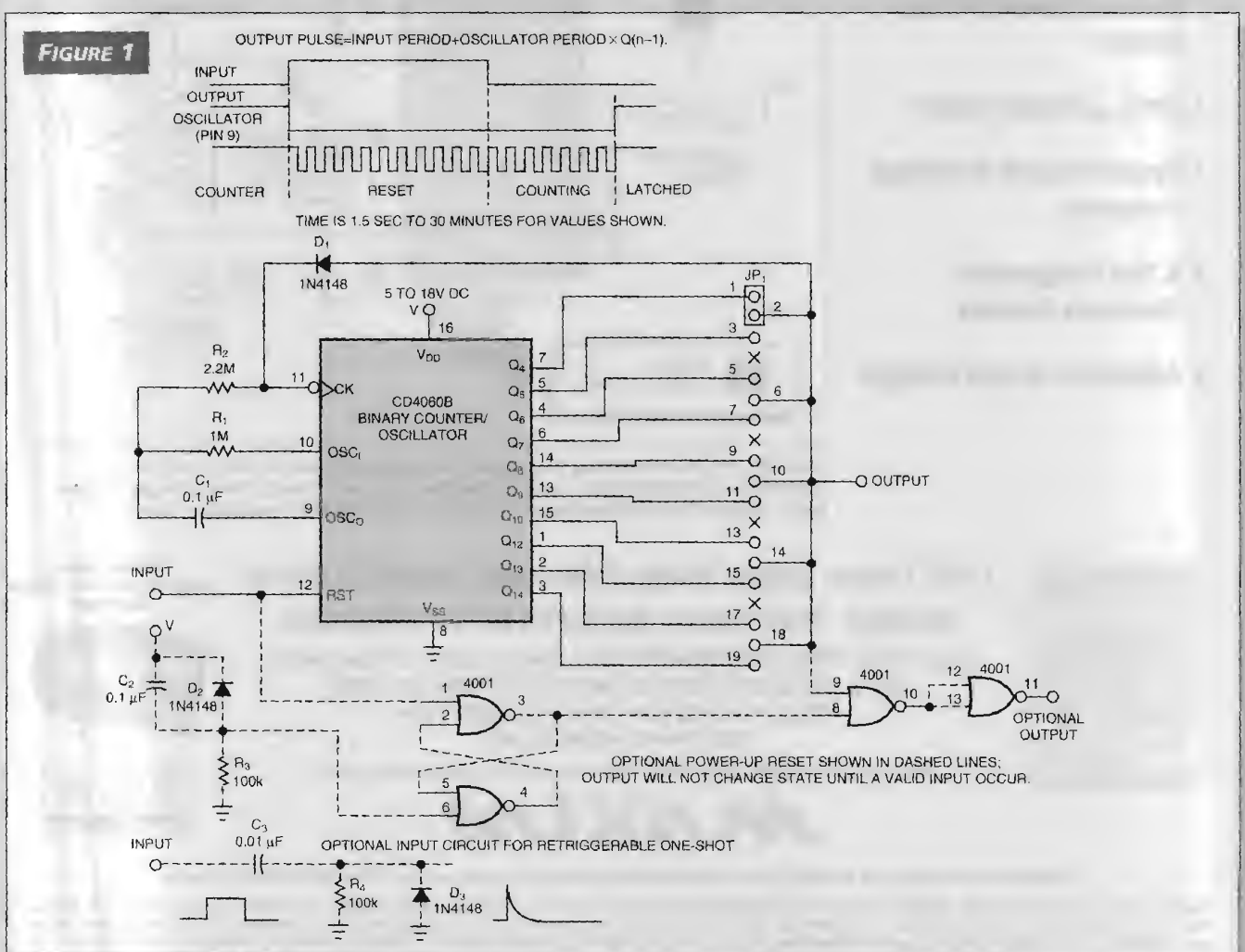
FIGURE 1



A low-cost logic IC is the heart of an accurate, long-delay timer. The circuits with broken lines offer options for power-up reset or for configuring a retriggerable one-shot multivibrator.

Variable-gain stage uses voltage-output DAC

EUGENE PALATNIK, BCI INTERNATIONAL, WAUKESHA, WI

A voltage-output DAC normally generates an output voltage that is a fraction of the input-reference voltage. In many designs, however, it is necessary to multiply the input voltage by a programmable gain, or, in other words, to create a variable-gain stage. You can easily implement a variable-gain stage using a low-cost voltage-output DAC (Figure 1). IC_1 includes three independent DACs, two of which have internal buffers. This design uses the third DAC (DAC C with output OUT_C) for the variable-gain stage. This no-buffer design minimizes noise and voltage offset, but you can use buffered DACs, too. Various linearity tests reveal a maximum nonlinearity error of 13.2 mV, which is less than the ±1-LSB (±19.5-mV) integral nonlinearity of the MAX512.

The output voltage of the DAC, V_{DAC}, is as follows, where N is the code clocked into the DAC:

$$V_{DAC} = \frac{V_{REF} \bullet N}{256}.$$

IC_{2A} compares V_{DAC} with V_{IN}. To close the feedback loop, the output of IC_{2A} connects to DAC C's voltage-reference input, REF_C. In steady-state mode, $V_{IN}=V_{DAC}$, and, because $V_{REF}=V_{OUT}$,

$$V_{OUT} = \frac{V_{IN} \bullet 256}{N}.$$

When N equals its maximum value of 255, the gain of the circuit equals 1.004. The maximum practical gain is at N=1, which equates to a gain of 256. R_1 and C_1 reduce the loop gain as the frequency increases, which helps make the circuit stable and reduces the bandwidth and overall noise.

An 80C51 µC controls the DAC using a three-wire-plus-reset interface. The µC serially clocks the gain value in the DAC while the SELECT line is low. Pulling SELECT high sets the new gain value. Because the DAC and op amp are rail-to-rail parts, the circuit can operate in rail-to-rail mode. The DAC itself is not critical; you can use voltage-output DACs with external-reference inputs from different vendors. (DI #2055) EDN

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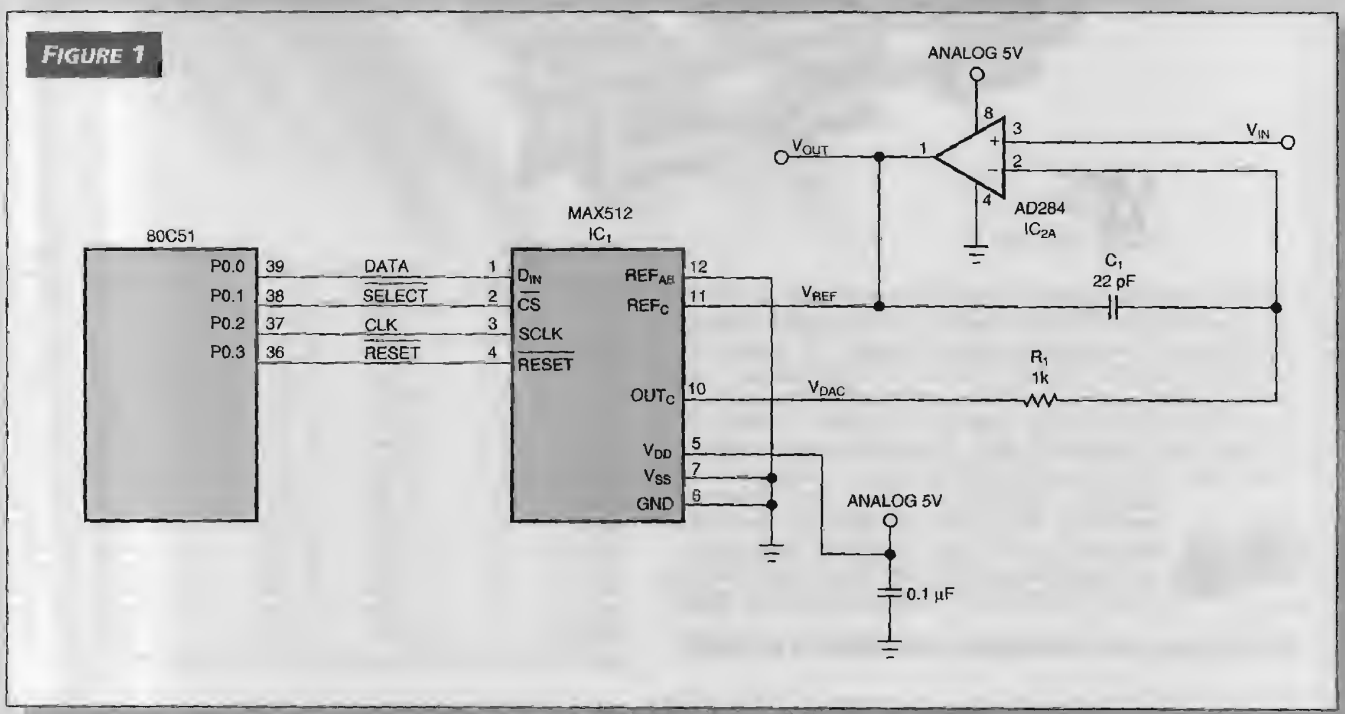
FIGURE 1



By comparing the DAC output voltage (V_{DAC}) with V_{IN}, you can easily implement a variable-gain stage using a low-cost voltage-output DAC.

the series resistor should be size 1206. The series resistor adds a propagation delay of 80 nsec on the rising edge and 60 nsec on the falling edge.

74HC outputs also benefit from the spark gap. Combined with generic silicon clamping diodes to V_{CC} and ground, a 100Ω series resistor protects a National 74HC14 output from dozens of 25-kV ESDs. A 47Ω resistor did not protect the sample part as well, causing a failure after only one or two 25-kV discharges. You need to carefully evaluate the value of the series resistor for each application.

Finally, as with RS-232C drivers, RS-485 drivers cannot take advantage of the spark gap. You must protect these drivers with Transzorbs, one on each line to ground. Two Motorola MMBZ15VVDLT1 Transzorbs protected a National 36C278 driver against dozens of 25-kV discharges. (DI #2072) EDN

To Vote For This Design, Circle No. 427

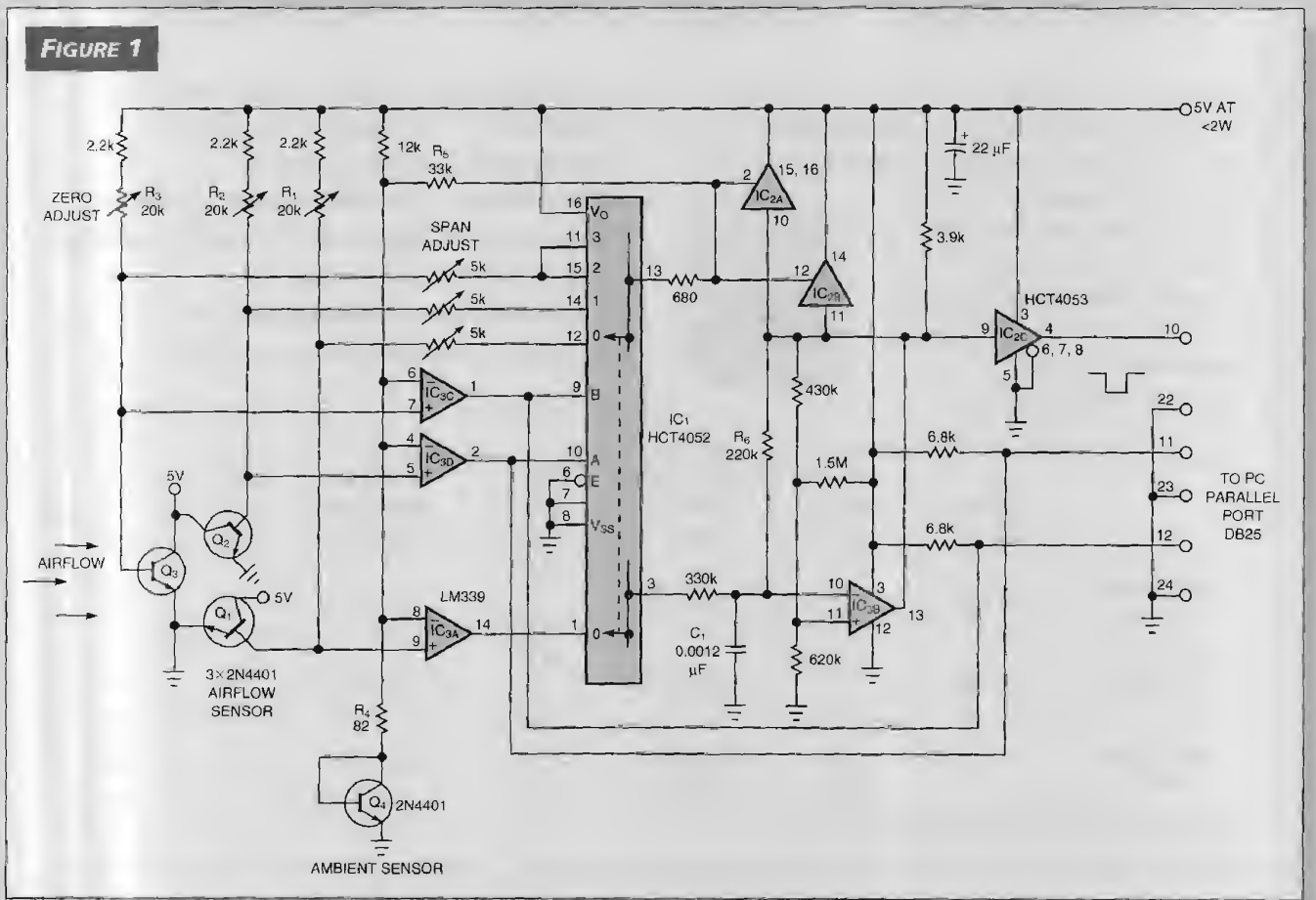
Transistor trio makes vector anemometer

W STEPHEN WOODWARD, CHEMISTRY DEPARTMENT, UNIVERSITY OF NORTH CAROLINA—CHAPEL HILL
WOODWARD@NET.CHEM.UNC.EDU

A previously published Design Idea (Reference 1) uses a heated transistor as an airspeed-to-frequency converter. Because it uses only one transistor, the circuit cannot determine the direction of airflow. Alternatively, a circuit that uses a trio of hot transistors can digitize both wind speed and direction (**Figure 1**).

The basic principle of operation is identical to that of the previous circuit. In the zero-airflow case, zero-adjust potentiometers R_1, R_2, and R_3 set quiescent bias currents for self-heated transistors Q_1, Q_2, and Q_3, respectively. If you properly adjust the resistors, collector power dissipation causes a still-air temperature rise in the transistor sensors of approximately 50°C, which in turn reduces the sensors' V_{BE}s by approximately 2 mV/° to just slightly below Q_4's V_{BE} plus the drop across R_4. Then, the voltages at the noninverting inputs of comparators IC_{3A}, IC_{3C}, and IC_{3D} are slightly lower than

FIGURE 1



Q_1 to Q_3 comprise an airflow sensor that enables the circuit to digitize both wind speed and direction.

the voltages at their inverting inputs. These comparators' outputs therefore go low, holding C_1 discharged and multivibrator IC_{3B} reset with its output high. This action causes a zero-frequency output on IC_{2C} and holds IC_{2A} and IC_{2B} off.

If a nonzero airflow impinges on the sensor array, the resulting increase in cooling rate tends to raise the airflow sensor's V_{BE} relative to Q_4's V_{BE}. This change reverses the voltage relation at one or more comparator input pairs and releases the reset on C_1. C_1 then charges through R_6 until the voltage at IC_{3B}'s inverting input is greater than the voltage at its noninverting input, causing IC_{3B}'s output to snap low, beginning the discharge of C_1 through R_6 and turning on IC_2. IC_1 now directs an approximately 700-µsec pulse through the span-adjust-potentiometer array to whichever sensor transistor triggered the cycle. The resultant pulse of collector current deposits a quantum of heat tending to warm that sensor's temperature enough to restore the original zero-flow voltage balance with Q_4. Until that temperature is restored, IC_{3B} continues to oscillate and cycle on IC_2. This feedback loop acts to maintain a constant temperature differential among sensors Q_1 to Q_3 and Q_4. The frequency at IC_{3B}'s output is therefore proportional to the extra power required to heat the array and thus directly related to airspeed.

Meanwhile, feedback through R_5 latches the address of the sensor transistor whose cooling triggered the cycle, so only that transistor receives the heating pulse. This binary (0, 1, or 2) sensor address is available at the output. Thermal coupling between the sensors depends on airflow direction. In **Figure 1**, for example, Q_3 is the most upwind sensor and is therefore the most strongly cooled. This effect is the basis for the computation of wind angle (see Basic program on *EDN*'s Web site, www.ednmag.com. To download the program, go into the Software Center and download the file from DI-SIG, #2073).

The anemometer's output is suitable for direct connection to the parallel port of a desk or laptop PC. You can then run the accompanying Basic program to report wind speed and direction once per second.

The maximum output frequency for the circuit as shown is 1 kHz. Appropriate adjustment of the span-adjust potentiometers establishes almost any desired full-scale flow rate from less than 1 to greater than 10 m/sec (which is equivalent to less than 2 to greater than 20 knots.) Response time is less than 2 sec because of the constant-temperature operation of the sensors. Tracking among Q_1, Q_2, Q_3, and Q_4 compensates for changes in ambient temperature. The circuit operates from one 5V power source. Power consumption depends on airflow rates but is typically less than 2W. (DI #2073) EDN

Reference

1. Woodward, W Stephen, "Self-heated transistor digitizes airflow," *EDN*, March 14, 1996, pg 86).

To Vote For This Design, Circle No. 428

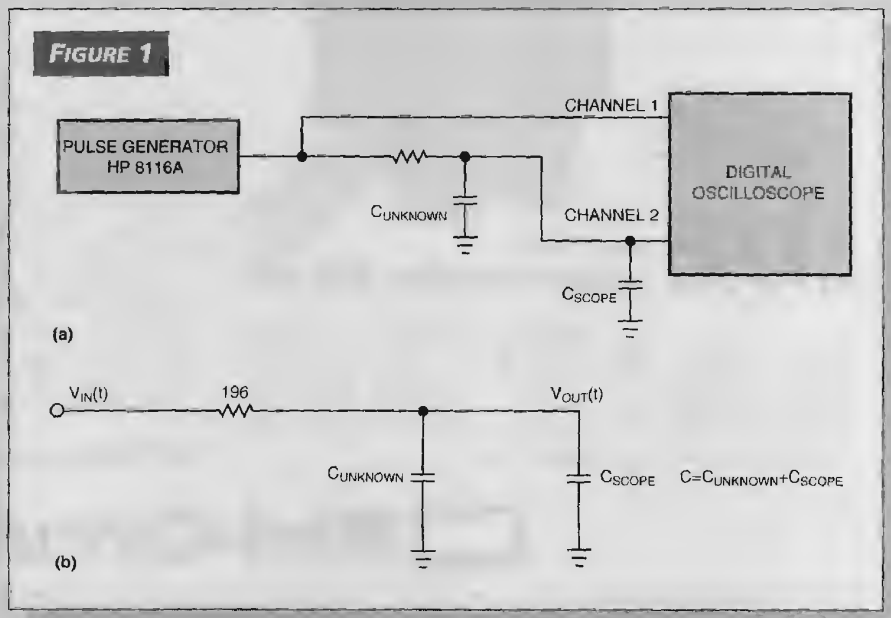
Simple technique measures small capacitance

RICH KOCHIS AND JOE ECCHER, HEWLETT-PACKARD, GREELEY, CO

A simple technique (**Figure 1**) can measure small capacitance, such as the capacitance of a scope probe (**Figure 3a**), a 10-pF capacitor (**Figure 3b**), and a pc-board trace (**Figure 3c**). The idea is to use a ramp generator and an oscilloscope (**Figure 1a**) to measure the delay in the ramp that corresponds to the capacitance. Equations provide the best explanation of how the tech-

A simple technique to measure small capacitance uses only a ramp generator, an oscilloscope, and some passive components (a). The unknown capacitance is one element in the network (b) that drives channel 2 of the scope. ▶

FIGURE 1



nique works. For the circuit in **Figure 1b**, which drives channel 2 of the oscilloscope,

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{1/sC}{R+1/sC} = \frac{1}{sRC+1}.$$

Thus,

$$V_{OUT}(s) = \frac{V_{IN}(s)}{sRC+1}.$$

V_{IN} is a ramp, so

$$V_{IN}(t) = Kt, \quad (1)$$

and

$$V_{IN}(s) = \frac{K}{s^2}.$$

Therefore,

$$V_{OUT}(s) = \frac{K}{s^2(sRC+1)} = KRC\left(\frac{1}{s^2RC} - \frac{1}{s} + \frac{RC}{sRC+1}\right),$$

and

$$V_{OUT}(t) = KRC\left(\frac{t}{RC} - 1 + e^{-t/RC}\right).$$

For T>>RC,

$$V_{OUT}(t) = KRC\left(\frac{t}{RC} - 1\right), \quad (2)$$

and $V_{IN}(t)$ and $V_{OUT}(t)$ become two parallel lines (**Figure 2**). From **Equation 1**,

$$T_1 = \frac{V_{IN}(t)}{K},$$

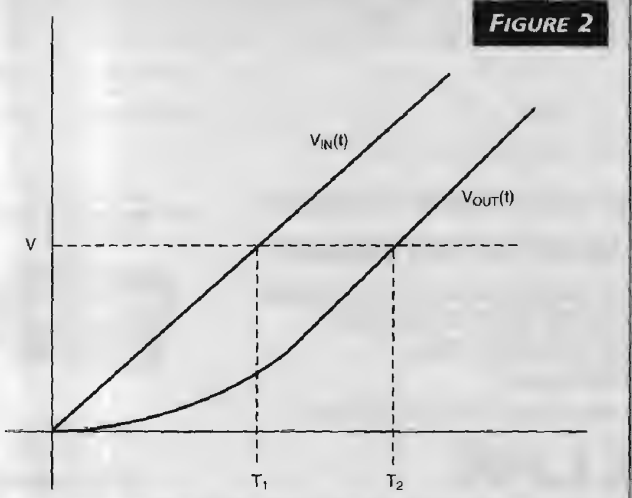
and from **Equation 2**,

$$V_{OUT}(T_2) = KRC\left(\frac{T_2}{RC} - 1\right) = KT_2 - KRC.$$

Thus,

$$T_2 = \frac{V_{OUT}(T_2) + KRC}{K}.$$

FIGURE 2



When T>>RC, where $C=C_{UNKNOWN}+C_{SCOPE}$, $V_{IN}(t)$ and $V_{OUT}(t)$ become two parallel lines and $C=\Delta T/R$.

You can define ΔT as

$$\Delta T = T_2 - T_1 = \frac{V_{OUT}(T_2) + KRC}{K} - \frac{V_{IN}(T_1)}{K}.$$

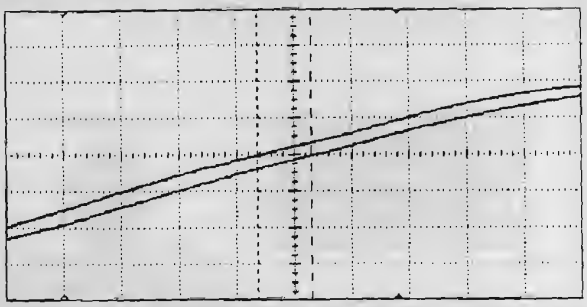
For the voltage at which $V_{IN}(T_1)=V_{OUT}(T_2)$ and when T>>RC,

$$\Delta T = RC.$$

Thus,

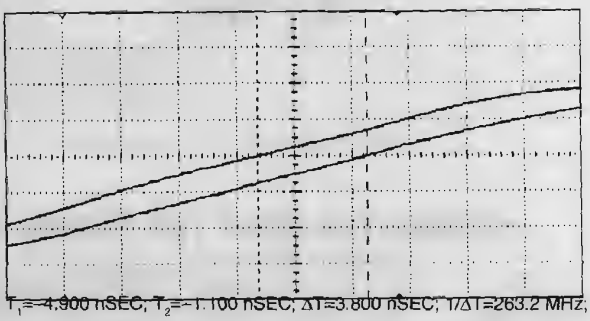
$$C = \frac{\Delta T}{R},$$

FIGURE 3



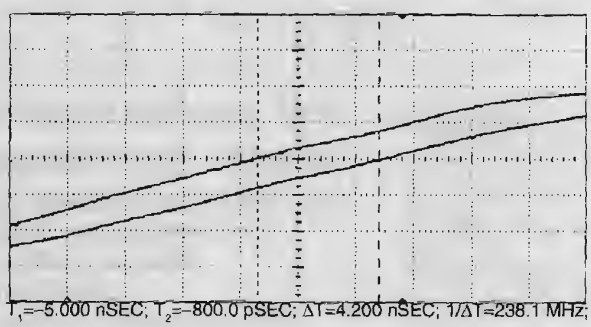
T_1=–4.900 nSEC; T_2=–3.000 nSEC; ΔT=1.900 nSEC; 1/ΔT=526.3 MHz;

(a) $C_{SCOPE} = \frac{1.90\times10^{-9}}{196} = 9.7$ pF.



T_1=–4.900 nSEC; T_2=–1.100 nSEC; ΔT=3.800 nSEC; 1/ΔT=263.2 MHz;

(b) $C_{10\ pF} = \frac{(3.8-1.9)\times10^{-9}}{196} = 9.7$ pF.



T_1=–5.000 nSEC; T_2=–800.0 pSEC; ΔT=4.200 nSEC; 1/ΔT=238.1 MHz;

(c) $C_{UNKNOWN} = \frac{(4.2-1.9)\times10^{-9}}{196} = 12$ pF.

Measuring the capacitance of a scope probe (a), a 10-pF capacitor (b), and a pc-board trace (c) is as easy as measuring ΔT.

where

$$C_{UNKNOWN} = C - C_{SCOPE}.$$

Therefore, C depends only on ΔT and R (when T>>RC), and C is independent of the slope, K, and voltage level. To measure T, you must only make sure that the voltage slopes are parallel, which is the case when T>>RC. The oscilloscope's capacitance is included in the reference-voltage measurement of T_1. Therefore, the unknown capacitance is the variable in the measurement of T_2 divided by R. (Note that if the unknown C measurement includes an input to an IC, you need to limit the input ramp voltage to less than 0.5V.) (DI #2075) EDN

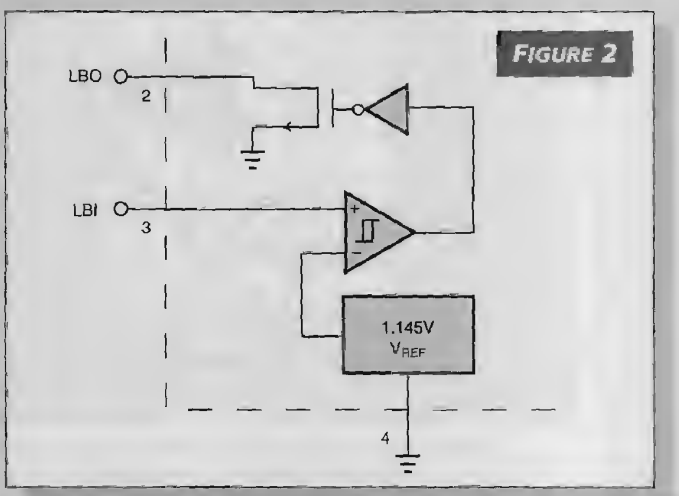
To Vote For This Design, Circle No. 429

Coilless step-up converter yields dual outputs

SAM NORK, LINEAR TECHNOLOGY CORP, BURLINGTON, MA

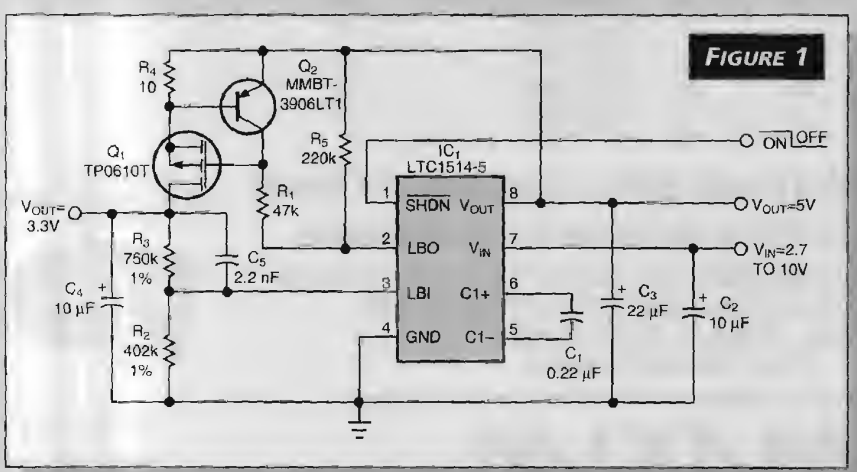
Rapidly proliferating battery-powered systems create a need for dc/dc converters that can accommodate a wide input-supply range. Depending on the battery-pack configuration, the input-supply voltage may be higher or lower than the desired regulated output voltage. The circuit in **Figure 1** provides regulated 5 and 3V supplies from a wide input range without the need for inductors. The LTC1514-5 (IC_1) is a switched-capacitor, step-up/step-down dc/dc converter. It produces a regulated 5V±4% supply capable of sourcing as much as 50 mA of output current. The circuit requires only three external capacitors to produce 5V from an input supply of 2.7 to 10V.

IC_1 draws a low, 60-μA-typical quiescent current. For a 3V input, the conversion efficiency for the 5V output ranges from 70% at a 0.5-mA output to 81% at a 50-mA output. For a 6V input, these efficiency figures become 71.5 and 82.5%, respectively. IC_1 contains a low-battery comparator that serves as a feedback comparator to create an auxiliary 3.3V supply (**Figure 2**). IC_1's internal reference connects to one end of the feedback comparator. The R_2-R_3 feedback voltage divider establishes the output voltage. The output of the comparator enables the current source comprising Q_1, Q_2, R_1, and R_4.



The low-battery comparator in the LTC1514-5 and a handful of external components collaborate to produce a regulated 3.3V output.

When the LBO output is low, Q_1 turns on, allowing current to charge output capacitor C_4. Local feedback formed by R_4, Q_1, and Q_2 creates a constant-current source from the 5V output to C_4. R_4 and Q_2's V_{BE} set the peak charging current. R_4 and Q_2's V_{BE} also provide current limiting in the case of an output short circuit to ground. IC_1 also protects the 5V output against short circuits. R_5 pulls Q_1's gate high when the 3.3V output is in regulation, thereby turning off the C_4 charging current. C_5 reduces output ripple.



Battery-powered equipment using both 3.3 and 5V can use this easy-to-implement dual-output dc/dc converter. The converter uses no inductors and accepts a 2.7 to 10V input range.

Because the auxiliary regulator implements a hysteretic feedback loop in place of the traditional feedback loop, the circuit needs no compensation for loop stability. Furthermore, the high gain of the comparator provides excellent load regulation and transient response. With the values in **Figure 1**, the dual regulator delivers a maximum combined output current of 50 mA. (DI #2076) EDN

To Vote For This Design, Circle No. 430

Isolated telecomm converter handles 25W

RON YOUNG, MAXIM INTEGRATED PRODUCTS, SUNNYVALE, CA

Many telecomm applications in the central office require an isolated 5V supply derived from –48V. The circuit in Figure 1 inserts an isolated, high-bandwidth feedback circuit into the loop of a transformer-flyback switching converter, IC_1, configured to generate 5V at 5A from an input voltage of –36 to –72V. Primary transformer T_1 provides isolation in the forward direction. An isolated transformer driver, IC_2, in conjunction with a surface-mount transformer, T_2, converts the isolated 5V output to a voltage that's referred to the primary and proportional to 5V.

The diode bridge comprising D_3, D_4, D_7, and D_8 converts the transformer output to dc. A diode-resistor network (D_2, R_4, and R_5) compensates for the temperature coefficient of the diode bridge. The result is a voltage with zero temperature coefficient, slightly lower than half the fed-back isolated 5V. IC_2 operates with inputs from 3 to 6V. For 5V output, the feedback voltage at Pin 3 of IC_1 is 2.404V. At 100 kHz (much greater than the loop bandwidth), the delay through the feedback circuit equates to a 9° phase shift. Supply current for the feedback circuit is approximately 6 mA, including the load of the temperature-compensation network.

To accommodate the isolated feedback circuit, the only modification you need to make on a nonisolated converter is to reduce the value of R_2 such that the R_2-R_3 voltage divider matches the 1.5V reference voltage internal to IC_1. You should trim R_2 in production to compensate for turns-ratio variations in T_2, unless an initial tolerance of 5 to 10% is acceptable. For 1% initial tolerance, trimming is mandatory regardless of the feedback technique. The transformer provides isolation to 500V rms; ratings to 1500V rms are also available. The converter delivers an isolated 5V at 5A with efficiency greater than 80%. For load currents of 0 to 5A, regulation is approximately 2%. For input voltages of –36 to –65V, the line regulation is better than 1%. (DI #2082)

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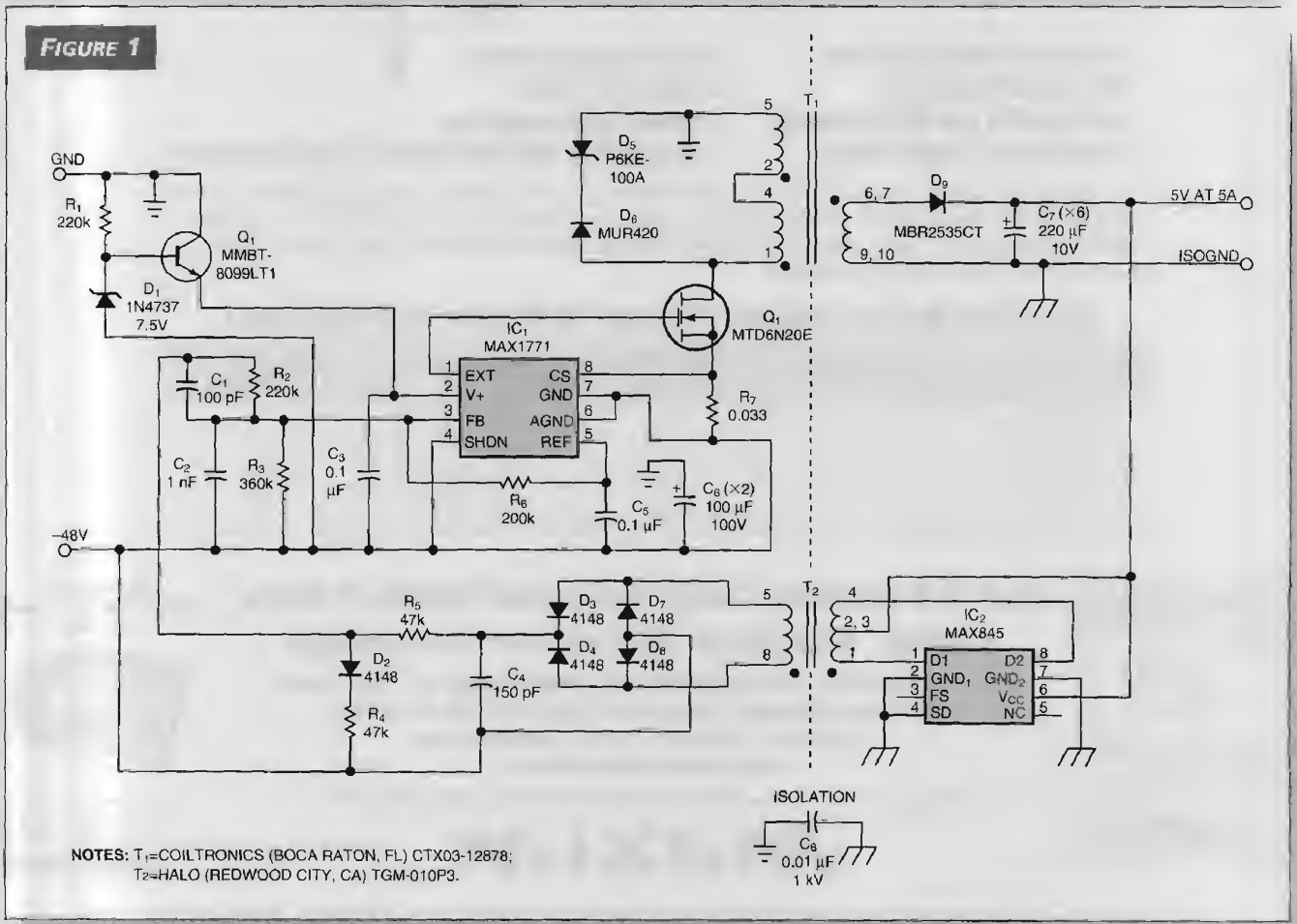
FIGURE 1



NOTES: T1=COILTRONICS (BOCA RATON, FL) CTX03-12878; T2=HALO (REDWOOD CITY, CA) TGM-010P3.

This –48 to +5V isolated flyback converter illustrates the use of a separate transformer for isolation of the feedback signal.